

In re Patent Application of
RAYNOR
Serial No. 10/645,320
Filed: AUGUST 21, 2003

REMARKS

Applicant again thanks the Examiner for the careful and thorough examination of the present application, and for the indication of allowable subject matter. By this amendment, Claims 14, 29 and 43 have been amended to include subject matter of respective dependent Claims 25, 39 and 49 which have now been canceled. Claims 26, 40 and 50 have been amended to include the subject matter of their respective independent claims, and are now in condition for allowance as indicated by the Examiner. Various claims have been amended for consistency with the above mentioned amendments. Claims 14-24, 26-38, 40-48, 50 and 51 remain pending in the application. Favorable reconsideration is respectfully requested.

I. The Invention

As shown in FIGS. 3 and 4, for example, the disclosed invention is directed to a solid state image sensor and method including an active pixel image sensor being formed on a P-type epitaxial layer on a P-type substrate. An active pixel array is in the P-type epitaxial layer. Each pixel includes an N-well functioning as a collection node, and a P-well adjacent the N-well. The pixels include only NMOS transistors functioning as active elements. The in-pixel transistors cooperate with off-pixel PMOS transistors to form A-D converters. Circuit elements that are external to the active pixel array include a respective comparator and counter for each pixel.

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II. The Claims are Patentable

Claims 14-19, 21, 22, 25, 29-33, 35, 36, 39, 43-45 and 47-49 were rejected in view the disclosed prior art discussed in the background section and illustrated in FIGs. 1 and 2 of the present application, in combination with Watanabe (US Patent No. 6,448,104) for the reasons set forth on pages 2-7 of the Office Action. The subject matter of Claims 20, 23, 24, 26-28, 34, 37, 38, 40-42, 46, 50 and 51 was indicated as being allowable. As mentioned above, independent Claims 14, 29 and 43 have been amended to include subject matter of respective dependent Claims 25, 39 and 49 which have now been canceled. Claims 26, 40 and 50 have been amended to include the subject matter of their respective independent claims, and are now in condition for allowance as indicated by the Examiner. Applicant contends that Claims 14-19, 21, 22, 29-33, 35, 36, 43-45 and 47, 48 clearly define over the cited art, and in view of the following remarks, favorable reconsideration of the rejections under 35 U.S.C. §103 is requested.

Each of the independent Claims 14, 29 and 43 recites that each pixel comprises a first well of a second conductivity type functioning as a collection node, and at least one second well of the first conductivity type adjacent the first well. Importantly, each pixel comprises a plurality of MOS transistors of only the second conductivity type functioning as active elements of the pixel. Circuit elements that are external to the active pixel array include a

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respective comparator and counter for each pixel. It is this combination of features which is not fairly taught or suggested in the cited art and which patentably defines over the cited art.

The Examiner has relied on the disclosed prior art discussed in the background section and illustrated in FIGs. 1 and 2 of the present application as teaching the use of a second well of the first conductivity type having NMOS transistors as active elements. However, the independent Claims 14, 29 and 43 have been amended to further include features of previously dependent Claims 25, 39 and 49 respectively. Specifically, these independent claims have been amended to recite circuit elements that are external to the active pixel array and include a respective comparator and counter for each pixel.

In the Office Action the Examiner states that the Applicant's prior art as shown in figures 1 and 2 of the present application discloses a solid state image sensor further comprising circuit elements external said active pixel array, said external circuit elements comprising respective comparator and counter for each pixel. However, it is submitted that this feature is not in fact disclosed in figures 1 and 2. In figure 2, the pixel is denoted by reference numeral 20 and includes all elements within the dotted line. These elements include NMOS transistors M1-M4 and a comparator formed by PMOS transistors M5-M7 and NMOS transistor M8. These transistors are part of the pixel and therefore cannot be said to be external said pixel array.

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Figure 4 of the present application illustrates an example of the invention, and discloses an image sensor that is different from that of Figs. 1 and 2. In figure 4, the pixel is again denoted by reference numeral 20 and comprises the elements within the dotted line. It can be clearly seen that transistors M5-M7 are external to the pixel. This is clearly different from Figs. 1 and 2, and so it cannot be said the applicants admitted prior art discloses a solid state image sensor where the circuit elements are external the active pixel elements array said external circuit elements comprising respective comparative counters for each pixel.

Furthermore, having the comparator outside the pixel significantly increases the responsiveness of an image sensor to incident light. When the comparator transistors are inside the pixel, they are for example PMOS transistors, which then have to be in an N-well. For the PMOS transistors to operate, this N-well has to be held at a positive voltage (Vdd) so there is a reverse bias transistor/well. This has an unwanted side effect - the positive voltage of the N-Well attracts (photo generated) electrons to it. This therefore reduces the sensitivity of the pixel and the efficiency of the image sensor.

Additionally, Applicant points out that the supporting reference of Watanabe also does not disclose or teach the use of circuit elements that are external to the active pixel array and including a respective comparator and counter for each pixel, as claimed.

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As the Examiner is aware, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim features.

There is simply no teaching or suggestion in the cited art to provide the combination of features as claimed. Accordingly, for at least the reasons given above, Applicant maintains that the cited art does not disclose or fairly suggest the invention as set forth in Claims 14, 29 and 43. Furthermore, no proper modification of the teachings of this reference could result in the invention as claimed. Thus, the prior art rejection should be withdrawn.

It is submitted that the independent claims are patentable over the prior art. In view of the patentability of the independent claims, it is submitted that their dependent claims, which recite yet further distinguishing features are also patentable over the cited reference for at least the reasons set forth above. Accordingly, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. An early notice thereof is earnestly solicited.

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If, after reviewing this Response, there are any remaining informalities which need to be resolved before the application can be passed to issue, the Examiner is invited and respectfully requested to contact the undersigned by telephone in order to resolve such informalities.

Respectfully submitted,



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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 703-872-9306 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 23rd day of June, 2005.

